WHAT IS CLAIMED IS:

1. A charge pump comprising:

a first current mirror capable of injecting a first charging current, I(U), onto a loop filter coupled to an output of said charge pump and injecting a second charging current, I(U)/M, onto an integrator capacitor, wherein said first and second charging currents are controlled by a first common control signal such that said first charging current mirrors said second charging current by a factor M;

a second current mirror capable of draining a first discharging current, I(D), from said loop filter and draining a second discharging current, I(D)/M, from said integrator capacitor, wherein said first and second discharging currents are controlled by a second common control signal such that said first discharging current mirrors said second discharging current by said factor M;

a sampling circuit capable of coupling said second charging current and said second discharging current to said integrator capacitor so that said integrator capacitor is one of: i) charged and ii) discharged by a difference current between said second charging current and said second discharging current; and

a control circuit capable of detecting a voltage

difference between a voltage on said loop filter and a voltage on said integrator capacitor, wherein said control circuit is operable to adjust said first common control signal to minimize said voltage difference.

2. The charge pump as set forth in Claim 1 wherein said first current mirror comprises:

a first charging current source capable of injecting said first charging current onto said loop filter; and

a second charging current source capable of injecting said second charging current onto said integrator capacitor.

3. The charge pump as set forth in Claim 2 wherein said second current mirror comprises:

a first discharging current source capable of draining said first discharging current from said loop filter; and

a second discharging current source capable of draining said second discharging current from said integrator capacitor.

4. The charge pump as set forth in Claim 1 wherein said control circuit comprises an amplifier having a non-inverting input coupled to said integrator capacitor and an inverting input coupled to said loop filter.

5. The charge pump as set forth in Claim 4 wherein said first common control voltage is generated on an output of said amplifier.

6. The charge pump as set forth in Claim 1 wherein said control circuit, in response to an increase in voltage on said integrator capacitor, adjusts said first common control voltage so that said second charging current is reduced.

7. The charge pump as set forth in Claim 6 wherein said adjustment of said first common control voltage by said control circuit also reduces said first charging current.

8. The charge pump as set forth in Claim 1 wherein said control circuit, in response to a decrease in voltage on said integrator capacitor, adjusts said first common control voltage so that said second charging current is increased.

9. The charge pump as set forth in Claim 8 wherein said adjustment of said first common control voltage by said control circuit also increases said first charging current.

10. An integrated circuit comprising:

a system control section capable of operating at a plurality of clock speeds;

at least one of a phase-locked loop (PLL) and a delay-locked loop (DLL) capable of providing at least one clock signal to said system control section, said at least one of a PLL and a DLL comprising a charge pump, wherein said charge pump comprises:

a first current mirror capable of injecting a first charging current, I(U), onto a loop filter coupled to an output of said charge pump and injecting a second charging current, I(U)/M, onto an integrator capacitor, wherein said first and second charging currents are controlled by a first common control signal such that said first charging current mirrors said second charging current by a factor M;

a second current mirror capable of draining a first discharging current, I(D), from said loop filter and draining a second discharging current, I(D)/M, from said integrator capacitor, wherein said first and second discharging currents are controlled by a second common control signal such that said first discharging current mirrors said second discharging current by said factor M;

a sampling circuit capable of coupling said

second charging current and said second discharging current to said integrator capacitor so that said integrator capacitor is one of: i) charged and ii) discharged by a difference current between said second charging current and said second discharging current; and

a control circuit capable of detecting a voltage difference between a voltage on said loop filter and a voltage on said integrator capacitor, wherein said control circuit is operable to adjust said first common control signal to minimize said voltage difference.

11. The integrated circuit as set forth in Claim 10 wherein said first current mirror comprises:

a first charging current source capable of injecting said first charging current onto said loop filter; and

a second charging current source capable of injecting said second charging current onto said integrator capacitor.

12. The integrated circuit as set forth in Claim 11 wherein said second current mirror comprises:

a first discharging current source capable of draining said first discharging current from said loop filter; and

a second discharging current source capable of draining said second discharging current from said integrator capacitor.

13. The integrated circuit as set forth in Claim 10 wherein said control circuit comprises an amplifier having a non-inverting input coupled to said integrator capacitor and an inverting input coupled to said loop filter.

14. The integrated circuit as set forth in Claim 13 wherein said first common control voltage is generated on an output of said amplifier.

15. The integrated circuit as set forth in Claim 10 wherein said control circuit, in response to an increase in voltage on said integrator capacitor, adjusts said first common control voltage so that said second charging current is reduced.

16. The integrated circuit as set forth in Claim 15 wherein said adjustment of said first common control voltage by said control circuit also reduces said first charging current.

17. The integrated circuit as set forth in Claim 10 wherein said control circuit, in response to a decrease in voltage on said integrator capacitor, adjusts said first common control voltage so that said second charging current is increased.

18. The integrated circuit as set forth in Claim 17 wherein said adjustment of said first common control voltage by said control circuit also increases said first charging current.

19. A method of operating a charge pump, the charge pump comprising: 1) a first current mirror capable of injecting a first charging current onto a loop filter coupled to an output of the charge pump and injecting a second charging current onto an integrator capacitor, wherein the first and second charging currents are controlled by a first common control signal such that the first charging current mirrors the second charging current by a factor M; 2) a second current mirror capable of draining a first discharging current from the loop filter and draining a second discharging current from the integrator capacitor, wherein the first and second discharging currents are controlled by a second common control signal such that the first discharging current mirrors the second discharging current by the factor M, wherein the method comprises the steps of:

coupling the second charging current and the second discharging current to the integrator capacitor so that the integrator capacitor is one of: i) charged and ii) discharged by a difference current between the second charging current and the second discharging current;

detecting a voltage difference between a voltage on the loop filter and a voltage on the integrator capacitor; and

in response to the detection of the voltage difference, adjusting the first common control signal to minimize the voltage difference.

20. The method as set forth in Claim 19 wherein, in response to an increase in voltage on the integrator capacitor, the step of adjusting adjusts the first common control voltage so that the second charging current is reduced.

21. The method as set forth in Claim 20 wherein the step of adjusting also reduces the first charging current.

22. The method as set forth in Claim 19 wherein, in response to a decrease in voltage on the integrator capacitor, the step of adjusting adjusts the first common control voltage so that the second charging current is increased.

23. The method as set forth in Claim 22 wherein the step of adjusting also increases the first charging current.